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2-D Row-Column CMUT Arrays with an Open-Grid Support Structure

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***Abstract*—Fabrication and characterization of $64 + 64$ 2-D row-column addressed CMUT arrays with 250 µm element pitch and 4.4 MHz center frequency in air incorporating a new design approach is presented. The arrays are comprised of two wafer bonded, structured silicon-on-insulator wafers featuring an open-grid support structure on top of the CMUT plates, omitting the need for through wafer vias. A 5 mask process is used to produce 2-D row-column addressed CMUT arrays with 74 nm vacuum gaps, single crystalline silicon plates with optional lithographically defined mass loads, 120 V pull-in voltage, and high voltage insulation up to 310 V.**

I. Introduction

Capacitive micromachined ultrasonic transducers (CMUTs) require high electric field strengths in the order of 10^8 V/m to actuate the movable top plate in transmit operation and to increase its compliance in receive [1]. A prerequisite for achieving such high electric field strengths without using excessively high voltages is to have electrode gap spacings in the order of a couple of hundred nanometers. In the simplest possible CMUT design using direct fusion bonding, the oxide used for both structural support and insulation of the applied voltage has the same thickness as the vacuum gap [2]. As the theoretical dielectric breakdown field strength of silicon dioxide is roughly 10^9 V/m, even a few impurities in the oxide can degrade the breakdown strength enough to cause device failure [3]. Therefore, various designs have been suggested in the literature that seek to combine small vacuum gap spacings and extended structural posts able to withstand high voltages, e.g. through LOCOS oxidation or buried oxides [4], [5]. The latter process offers the highest degree of insulation, since the bottom electrode rests on a buried oxide (BOX) layer, the thickness of which can be chosen independently of the desired vacuum gap size. If such a process is used to fabricate fully populated 2-D arrays, through wafer vias are needed in order to access the bottom electrode [5]. This complicates the fabrication process considerably if the arrays are to be operated in the MHz range, where the via diameter is limited by the pitch of the closely spaced CMUT elements.

The purpose of this paper is to demonstrate a fabrication process primarily intended for row-column addressed 2-D arrays that benefit from the before mentioned insulation advantages of a buried oxide structure without the need for through wafer vias due to the use of an open-grid support structure. Row-column addressing has emerged as a promising addressing scheme for 2-D ultrasonic arrays, and it has been demonstrated theoretically that for three-dimensional imaging, the resolution and contrast of such arrays is comparable to fully addressed 2-D arrays [6], [7]. Prototypes of row-column addressed transducers using both CMUT technology [8], [9], and conventional bulk piezoelectric technology has been demonstrated, in the latter case in an impressive 256×256 size array with corresponding $256 + 256$ connections [10]. This paper exclusively covers the design and fabrication of the proposed structure, which is demonstrated on arrays with $64 + 64$ connections. Preliminary characterization tests are carried out to evaluate the basic performance of the design and to identify its strengths and weaknesses.

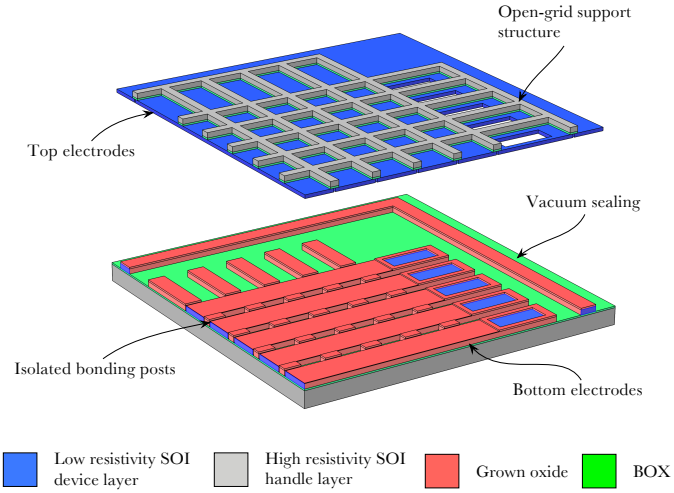


Fig. 1: An illustration of the 2-D row-column array design shown in exploded view with the top and bottom wafer separated at the bonding interface.

II. Design

The design presented in this paper is based on the criterion of having a highly insulating post structure, whilst still allowing for well-controlled vacuum gap sizes in the order of 100-200 nm. As covered in previous work in the literature, such a design can be realized using silicon-on-insulator (SOI) wafers with BOX layers that can support high voltages [5]. A second criterion is that the contact pads to the row- and column elements are accessible from the perimeter of the array. This criterion will allow for wire bonding to

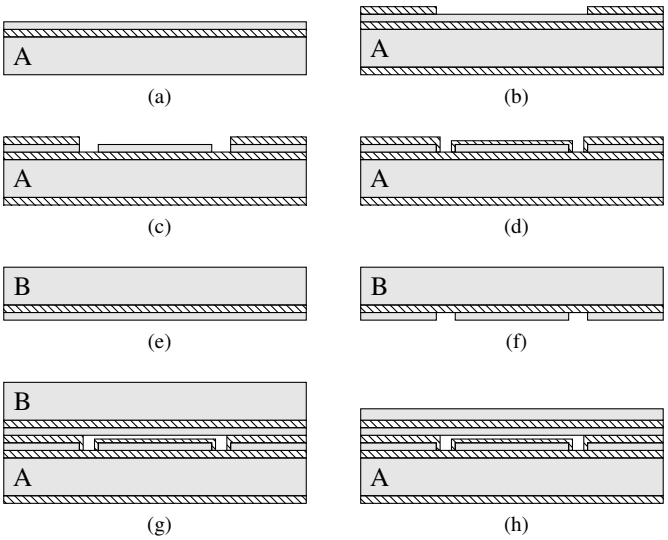


Fig. 2: An illustration of the main steps involved in the fabrication process. Silicon is illustrated in grey while silicon dioxide is shown in a striped pattern.

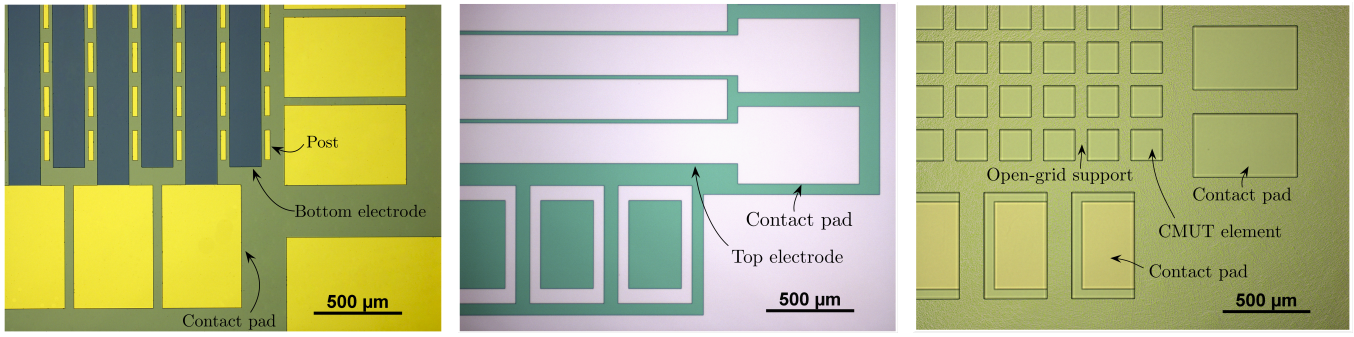
the front of the device without the need for through wafer vias, thereby simplifying the fabrication process considerably. Through wafer vias can, if desired, still be integrated for e.g. flip chip mounting. Finally, the flexural top plates of the CMUT elements should be made of single crystalline silicon to ensure uniform mechanical properties over large arrays. This dictates a wafer-bonding approach as originally suggested by Huang et. al [2] and used in later processes involving BOX insulation layers [5].

The listed requirements dictates a radical rearrangement of the mechanical structure supporting the flexible CMUT top plates. In Fig. 1, the proposed design is shown in exploded view with the device separated at the bonding interface. The bottom electrodes are resting on a BOX layer and are completely insulated from the top electrodes by either BOX layers or vacuum. Consequently, the isolated posts aligned parallel to the bottom electrodes can only ensure a well-defined gap between the top- and bottom plates. To define the individual CMUT elements, an alternative support structure is therefore needed to supply the mechanical support perpendicular to the bottom electrodes. The approach taken in this paper is to provide this through an open-grid support structure placed *above* the top electrodes, thereby allowing for top- and bottom electrodes insulated by BOX layers and vacuum. As seen in Fig. 1, the device is fabricated using two SOI wafers. Thus, the material for producing the open-grid support is supplied by the highly resistive handle layer and BOX layer of the top SOI wafer, enabling lithographical definition of the frame of the individual elements. The top electrodes are insulated from each other by etching trenches into the top SOI device layer. The vacuum gap between the top- and bottom electrodes is defined by having two accumulated oxide layers on the posts and only one on the bottom electrode as pull-in insulation, thereby ensuring precise control of the gap height. The vacuum is maintained through a vacuum sealing frame that surrounds the entire array.

A couple of important advantages of the open-grid support should be mentioned. First, since it is solely responsible for the definition of the CMUT elements, the bonding of the two wafers essentially only functions as vacuum sealing. All bonding interfaces are furthermore isolated from both top- and bottom electrodes. Thus, the bonding can, if desired, be carried out by alternatives to direct wafer bonding, e.g. eutectic bonding, which do not demand the same cleanliness and low surface roughness. In this paper, the design will be demonstrated using direct wafer bonding. A second major advantage of the open-grid support is the possibility of lithographically defining mass loads on the top plates together with the open-grid support. Additional mass loads can be desirable if high output pressures are wanted or if a more piston-like behavior of the CMUT top plate is needed [11], [12].

III. Fabrication

The main steps of the fabrication process are outlined in Fig. 2. A 4" silicon-on-insulator (SOI) wafer with a 2 µm low resistivity device layer, a 1 µm buried oxide layer (BOX), and a 500 µm high resistivity handle layer (wafer A) is used as the processing substrate for the bottom electrodes, see Fig. 2a. A 168 nm dry thermal oxide is grown and the device layer is patterned in a plasma etch through a lithographically defined resist mask using the silicon device layer as an etch stop as illustrated in Fig. 2b. A second lithography step is used to define a resist mask for a deep reactive ion etch through the device layer, this time with the BOX layer acting as etch stop, see Fig. 2c. The inductively coupled plasma etcher uses a low frequency 380 kHz generator in conjunction with the usual high frequency RF coil to avoid lateral etching or "notching" once the BOX is reached. As illustrated in Fig. 2d, a second 143 nm oxidation step follows, resulting in a total of 217 nm oxide in the post areas already containing oxide, ensuring both electrical insulation of exposed silicon surfaces and insulation of the bottom electrode during pull-in operation. Fig. 3a shows an optical micrograph of the resulting structure after this step. The yellow pads in the bottom of the figure are contact pads to the blue bottom electrodes, which are seen as vertical columns. Every second bottom electrode has a corresponding contact pad in the opposing end of the array. The colors are the actual colors of the different oxide layers, thereby clearly distinguishing the structures. As mentioned, the blue oxide covers the bottom electrodes as a result of the second oxidation. The yellow oxide is a product of both the first and the second oxidation, and will provide the bond surface during the direct wafer bonding step. Note the small rectangular posts in between the bottom electrodes, which will provide support for the crossing top electrodes. Each post is completely isolated on the underlying greenish BOX layer. In the bottom right corner, a part of the vacuum sealing frame illustrated in Fig. 1 is seen.



(a) (b) (c)

Fig. 3: Optical micrographs of the fabricated device. The bottom electrodes (a), top electrodes (b), and support grid (c) are all seen in the same corner section of a device, where both the electrodes and the bond pads can be seen. Every second bond pad is located at the opposing side of the array. In order to better visualize the alignment between the three layers, the micrograph of the top electrode (b) has been flipped around a vertical axis.

The top electrodes are etched into the device layer of a second SOI wafer (wafer B) as illustrated in Figs. 2e and 2f, once again using an ICP silicon etcher with a low frequency generator to avoid notching when the BOX layer is reached. The SOI wafer has a highly doped 20 µm device layer, a 1 µm BOX and a 500 µm lightly doped handle layer. Fig. 3b shows an optical micrograph of the result of this processing step. The shown area of the array corresponds to the area shown in Fig. 3a. Note, however, that since the wafer containing the top electrodes is to be bonded to the wafer containing the bottom electrodes, the image in Fig. 3b has been flipped around a vertical axis to better visualize the alignment of the structures. It is seen that the top electrodes are oriented perpendicularly to the bottom electrodes and that access is made to the bottom electrode contact pads through the top electrode device layer.

The two wafers are then cleaned using a standard RCA cleaning procedure, aligned to each other, and bonded at 50 °C for 5 minutes at 1500 N piston force and 10^{-2} mbar ambient pressure as illustrated in Fig. 2g (note that the top electrodes are not visible in this illustration as they are oriented perpendicularly to the bottom electrodes). The bonded wafers are subsequently annealed for 70 minutes at 1100 °C to increase the bonding strength. The handle layer of the SOI wafer containing the top electrodes is then thinned down in KOH at 90 °C, see Fig. 2h, having an etch rate of 1.57 µm/min. The etch rate is stable enough to allow precise thinning of the wafer to a desired thickness with a tolerance of roughly 2-4 µm. Thus, for the desired final handle thickness of 40 µm, a 36 µm thickness was realized in practice. Prior to the bonding, alignment marks had been etched into the handle of the SOI wafer containing the bottom electrodes. This alignment is used as back-to-front alignment in a lithography step on the thinned handle. The resulting resist mask acts as an etch mask in a subsequent ICP silicon etch using the BOX as a stop layer, in which the support structure and optionally mass loads are defined. Fig. 4 shows a SEM micrograph of a device having mass loads incorporated on the CMUT plates. The individual elements are designed for a resonant frequency in air of 7 MHz, dictating an active element side length of 180 µm. The exposed BOX as well as the underlying oxide on the bottom electrode contact pads are etched using an ICP oxide etcher, and the resulting structure after removing the resist mask can be seen in Fig. 3c, in this case with no mass loads. The slight reddish color on seen in the bottom electrode contact pads is due to the partial transparency of the 2 µm device layer. Note that the alignment during bonding is off by roughly 20 µm in the horizontal direction in Fig. 3c due to an issue with the bonding aligner in this direction. However, as this was a known issue, the margins in the design allows for up to 50 µm misalignment during bonding. The metal bond pads needed for wire bonding were not added to this prototype device, as this was not needed for the initial characterizations. Therefore, devices with wire bondings and individual external electrical connections are left for future batches. However, preliminary trials with the needed processing has been carried out, demonstrating the feasibility of patterning a resist over the elevated support structure if two independent resist spin-on steps are used. Alternatively, the metal pads can be incorporated in

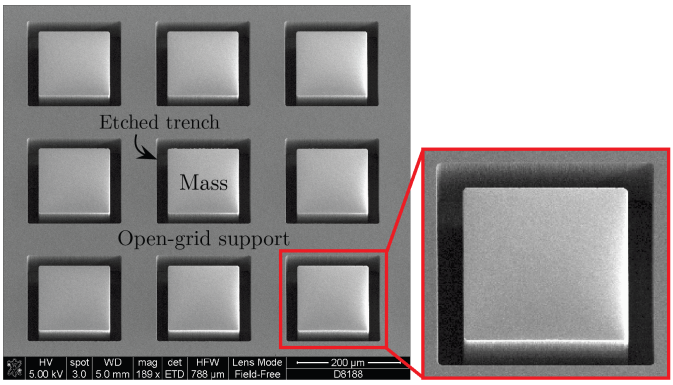


Fig. 4: SEM micrograph showing a detail of a device with lithographically defined and etched mass loads.

the bonding step by using eutectic bonding. As all bonding surfaces are isolated, and since the support grid is responsible for the structural support of the elements, a conductive eutectic bonding can be used with no disadvantage.

IV. Characterization

One of the main requirements of the device is its ability to withstand high voltages. Since all potentials are supported by BOX layers being 1 µm in thickness, the structure should, theoretically, withstand voltages up to 1000 V before breakdown occurs. In order to measure the actual breakdown voltage, a test structure was included on the chip which was identical to the CMUT elements, but with the handle still present on top of the plate. In this way, pull-in was avoided due to the much higher plate stiffness, hence allowing measurement of the breakdown voltage of the post. The measured breakdown voltage on this test structure was 310 V, i.e. considerably lower than the theoretical limit. This either suggests that the BOX oxide quality is poor or that surface currents are able to flow inside the device. The latter could be induced by alteration of the oxide surface during the reactive ion etching, where the ions can lead to trap formation. Despite the relatively low breakdown voltage of the posts compared to the theoretical limit, it is worth noting that this breakdown voltage is much higher than the measured pull-in voltage of the device, being 120 V. Therefore, the functionality of the additionally insulated post structure is verified.

The displacement frequency response of a single CMUT cell of the device for two different DC bias voltages was measured using laser Doppler vibrometry, and is shown in Fig. 5. The element was excited using a 10 V AC chirp signal, covering the frequency range in the vicinity of the resonant frequency in air. The resonant frequency is seen to be 4.4 MHz at a DC bias voltage of 80 V, dropping to just above 4.3 MHz at 110 V DC bias voltage due to the spring softening effect. This resonance frequency is roughly 3 MHz lower than a perfectly clamped rectangular plate of the same dimension as the CMUT element, indicating that the open-grid support structure is, as expected, not ideally rigid.

V. Conclusion

In this work, a new CMUT structure for 2-D row-column addressed arrays was proposed. The introduction of an open-grid support structure on top of the flexural plates enabled highly insulating post structures, the advantage of non-critical bonding, no need for through-wafer vias, and the possibility to integrate mass loads on the plates. The post structures could withstand up to 310 V, being significantly higher than the 120 V pull-in voltage of the device. Despite its demonstrated advantages, the open-grid support might lead to increased cross-coupling, and might have an effect on the acoustic output characteristics. These potential issues will be the subject of future research.

Acknowledgment

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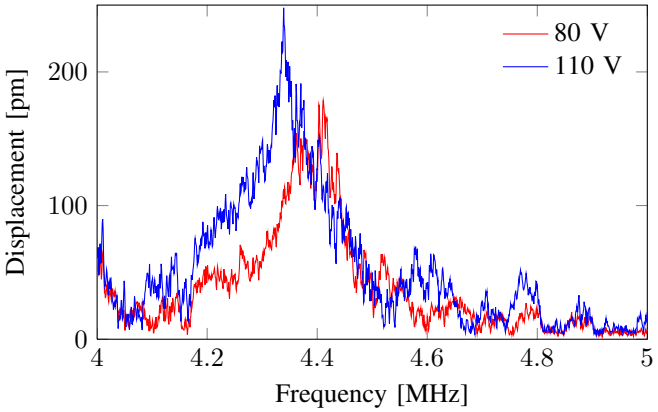

Fig. 5: Measurements of the top plate deflection as a function of frequency in the vicinity of the resonant frequency at two different bias voltages and an AC amplitude of 10 V. The measurements were recorded using laser Doppler vibrometry.

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